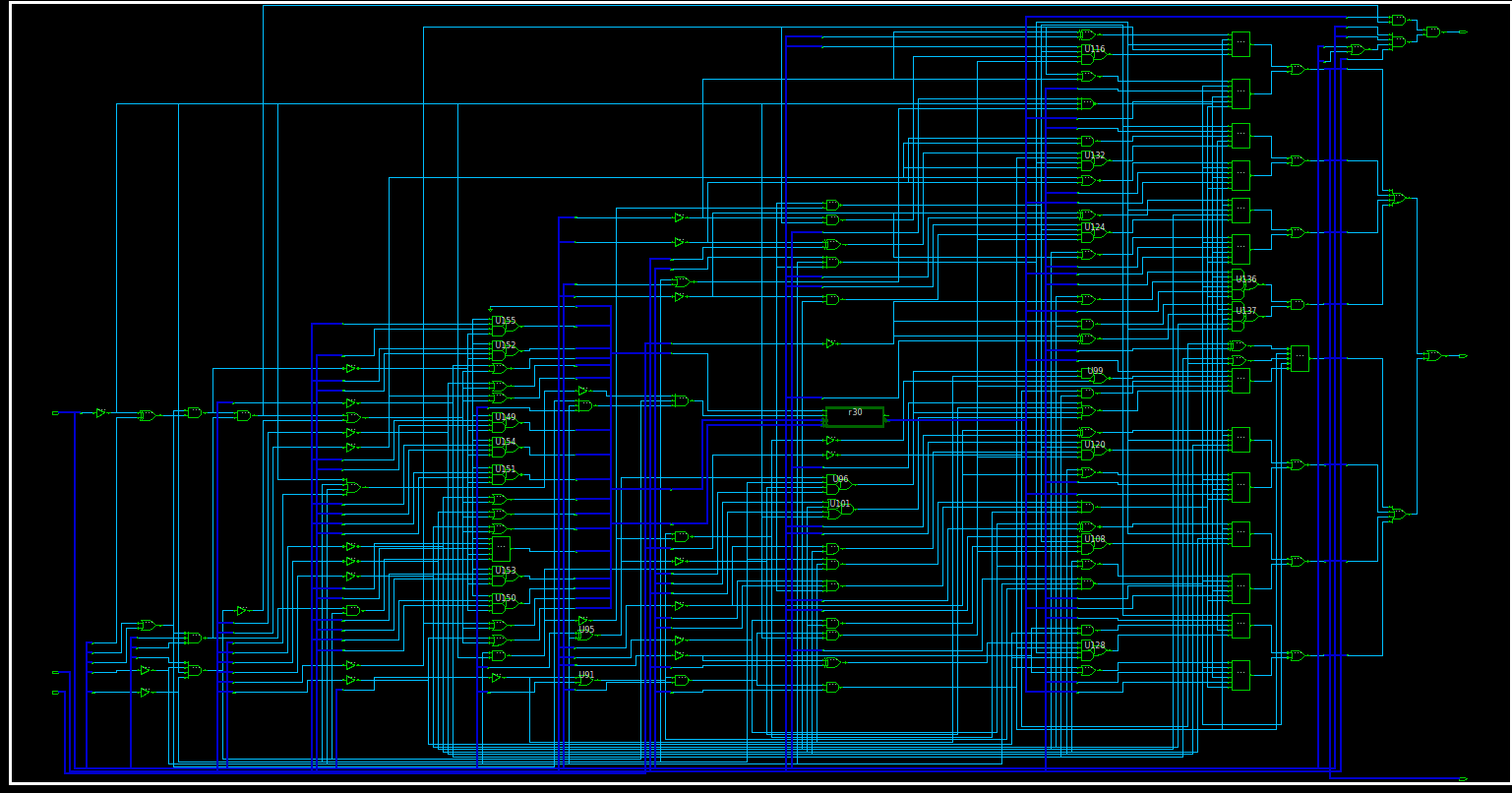
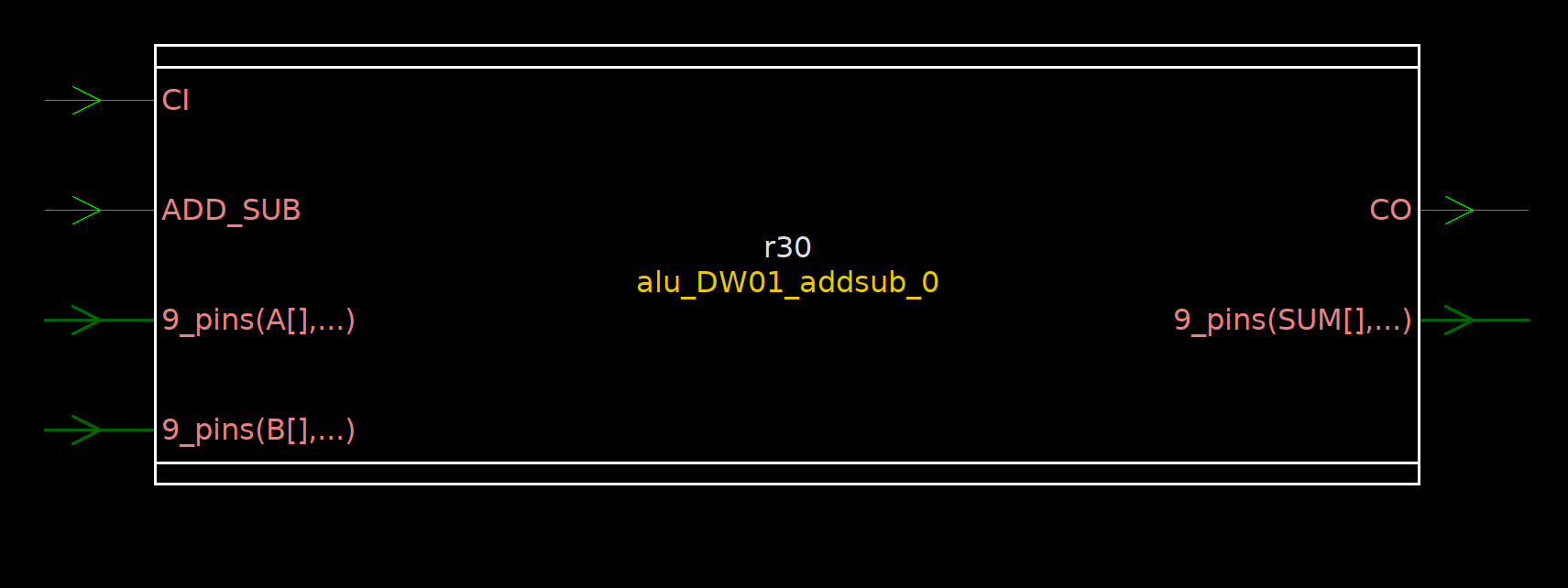
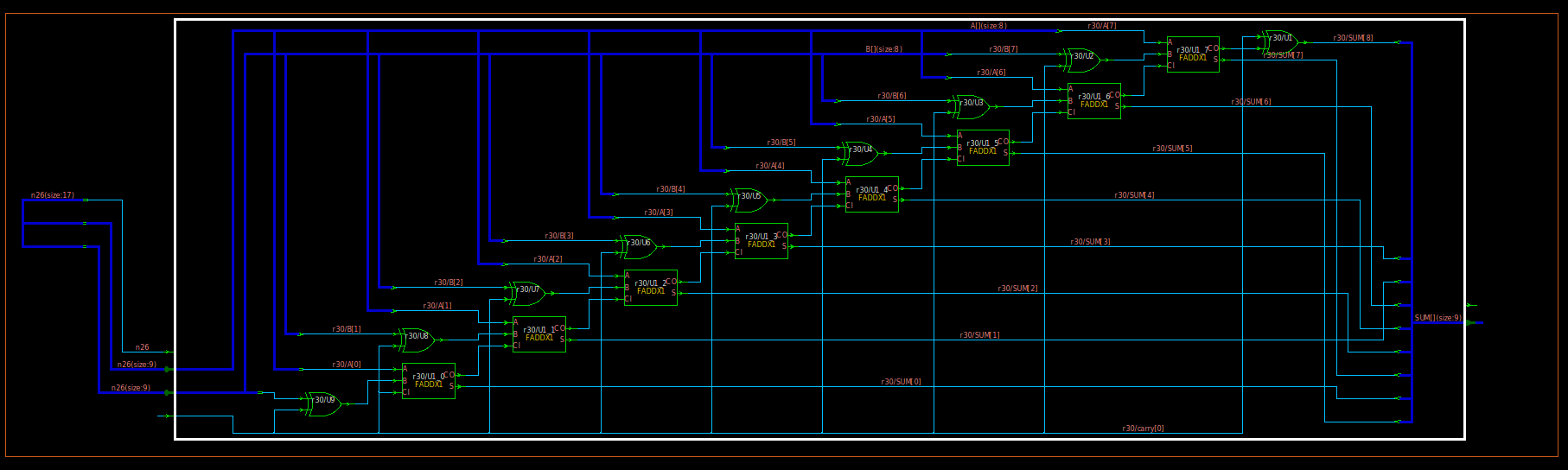
1. Your Verilog code
2. Turn in the schematic of your synthesized alu

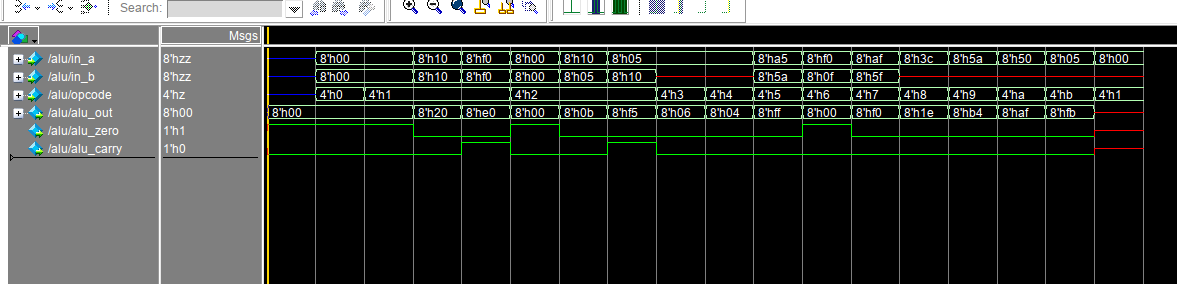








3. The waveform of your code working correctly at both RTL and gate levels.



ALU.do timing diagram from ModelSim

4) Now synthesize the RTL and produce the gate level design.

Determine the following and put your answers on a separate sheet:

1. Find the total area used by the alu. (report\_area command)

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : area

Design : alu

Version: L-2016.03-SP2

Date : Thu Apr 19 02:38:18 2018

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Information: Updating design information... (UID-85)

Library(s) Used:

saed90nm\_typ (File: /nfs/guille/a1/cadlibs/synop\_lib/SAED\_EDK90nm/Digital\_Standard\_Cell\_Library/synopsys/models/saed90nm\_typ\_pg.db)

Number of ports: 60

Number of nets: 204

Number of cells: 151

Number of combinational cells: 149

Number of sequential cells: 1

Number of macros/black boxes: 0

Number of buf/inv: 26

Number of references: 18

Combinational area: 1474.433013

Buf/Inv area: 143.780005

Noncombinational area: 0.000000

Macro/Black Box area: 0.000000

Net Interconnect area: 74.271335

**Total cell area: 1474.433013**

**Total area: 1548.704348**

1. How many different types of cells (gates) were utilized : (report\_hierarchy command)

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : hierarchy

Design : alu

Version: L-2016.03-SP2

Date : Thu Apr 19 02:52:00 2018

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

alu

AND2X1 saed90nm\_typ

AND3X1 saed90nm\_typ

AO21X1 saed90nm\_typ

AO22X1 saed90nm\_typ

AO221X1 saed90nm\_typ

AO222X1 saed90nm\_typ

AOI222X1 saed90nm\_typ

INVX0 saed90nm\_typ

NAND2X0 saed90nm\_typ

NAND3X0 saed90nm\_typ

NAND4X0 saed90nm\_typ

NOR2X0 saed90nm\_typ

NOR4X0 saed90nm\_typ

OA22X1 saed90nm\_typ

OR2X1 saed90nm\_typ

OR4X1 saed90nm\_typ

XNOR2X1 saed90nm\_typ

alu\_DW01\_addsub\_0

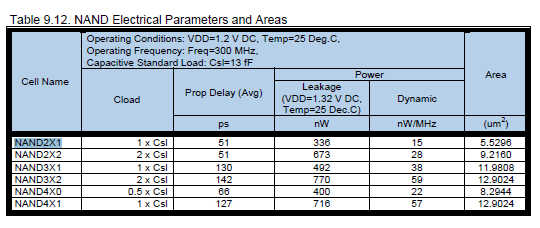
FADDX1 saed90nm\_typ

XOR2X1 saed90nm\_typ

**There were 19 different types of cells used**

c. Number of cells (gates). This will require using the report\_area command as well as looking at the cell library databook. It is located at:

/nfs/guille/a1/cadlibs/synop\_lib/SAED\_EDK90nm/Digital\_Standard\_Cell\_Library/doc/databook. Its is called SAED Digital Standard Cell library\_Rev1\_4\_20. Its is a pdf file but has no .pdf on it. Search for the cell "NAND2X1" and record the area. (pg 34) Divide the total area reported by design\_vision by this number to get the gate equivalent count.



Digital standard cell library for NAND including the NAND2X1

Gate Equivalent Area = 626.52 / 5.53 = **280 equivalent NAND gate count**.

d. The synthesis tool will most likely introduce a hierarchical block to your design because it recognized something in your design. What is the block and what does it do?

What style of implementation was chosen for this element?

Hint: see report\_hierarchy output

It created a 9 bit adder/subtractor using FADDX1(1-bit full adders and XOR2X1 (XOR’s). It is used in the arithmetic operations. It was created as a module which was instantiated into the ALU.

e. What was the maximum delay path through the alu and what were the beginning and endpoints for the max delay path?: (report\_timing command)

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 1

Design : alu

Version: L-2016.03-SP2

Date : Fri Apr 20 04:44:01 2018

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: TYPICAL Library: saed90nm\_typ

Wire Load Model Mode: enclosed

Startpoint: opcode[0] (input port)

Endpoint: alu\_zero (output port)

Path Group: (none)

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

alu 8000 saed90nm\_typ

alu\_DW01\_addsub\_0 8000 saed90nm\_typ

Point Incr Path

-----------------------------------------------------------

input external delay 0.00 0.00 r

opcode[0] (in) 0.00 0.00 r

U126/QN (INVX0) 0.19 0.19 f

U197/QN (NOR4X0) 0.54 0.72 r

U186/QN (INVX0) 0.12 0.84 f

U184/QN (NAND3X0) 0.38 1.22 r

r30/ADD\_SUB (alu\_DW01\_addsub\_0) 0.00 1.22 r

r30/U9/Q (XOR2X1) 0.22 1.44 r

r30/U1\_0/CO (FADDX1) 0.15 1.58 r

r30/U1\_1/CO (FADDX1) 0.13 1.72 r

r30/U1\_2/CO (FADDX1) 0.13 1.85 r

r30/U1\_3/CO (FADDX1) 0.13 1.98 r

r30/U1\_4/CO (FADDX1) 0.13 2.11 r

r30/U1\_5/CO (FADDX1) 0.13 2.25 r

r30/U1\_6/CO (FADDX1) 0.13 2.38 r

r30/U1\_7/S (FADDX1) 0.20 2.57 f

r30/SUM[7] (alu\_DW01\_addsub\_0) 0.00 2.57 f

U174/QN (AOI222X1) 0.23 2.81 r

U176/QN (NAND2X0) 0.08 2.89 f

U179/Q (OR4X1) 0.14 3.03 f

U177/QN (NOR2X0) 0.04 3.07 r

alu\_zero (out) 0.00 3.07 r

data arrival time 3.07

-----------------------------------------------------------

(Path is unconstrained)

**The total arrival time is 3.07 uS**